Implementation Of a Logic Expression in Different Levels of Abstraction to Determine Its Critical Voltages

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Abstract: In this work, the logic implementation of a boolean expression using vivado software is described in order to acquire an optimal gate level design and power analysis. Additionally, the LTSPICE circuit level abstraction is used to establish and implement the voltage transfer characteristics of this enhanced register transfer level architecture. The circuit is scaled down to an inverter level to aid with inspection. The power analysis and critical voltages are compared with the equation of the theoretical model to confirm the conclusions. Finally, using microwind, the relevant transistor's layout schematic is implemented. A variation in static and dynamic power of 220 mV and 10 mV, respectively, is seen in power analysis.

Index Terms: Gate-level, Circuit-level, Vivado, LTSPICE

I. INTRODUCTION

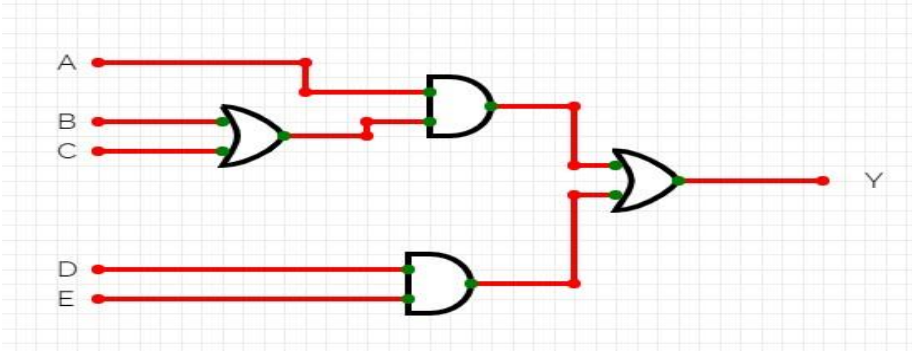
For the purpose of developing integrated circuits, VLSI design abstraction is essential. The two approaches that design engineers use to create integrated circuits (ICs) are top-down and bottom-up. Top-down design starts with the system level and moves to physical design, and vice versa for bottom-up design. By employing Hardware Description Languages (HDLs) like Verilog or VHDL to create designs, gate-level optimization may be accomplished. With the help of various design approaches, the optimized Register Transfer Level design may also be achieved at the circuit level. Because of the inherent benefits of static CMOS implementation, which include high packing density, increased functionality, reduced interconnection time, better noise margin, minimal steady-state power dissipation, and low influence of process fluctuations, it is commonly employed in most ICs. Additionally, by adhering to MOS Industry standards, the implementation of the circuit level may be done as layout diagrams. To find the inverter equivalent of a Boolean statement in CMOS and its theoretical Voltage Transfer Characteristics (VTC), use static CMOS logic. A brief introduction was offered in Section I, followed by sections that showed current works, the logic's implementation using Vivado and LTSPICE, and the layout design using Microwind. While the computations and findings are covered in Section IV, the conclusions are covered in Section V.

II. EXISTING WORK

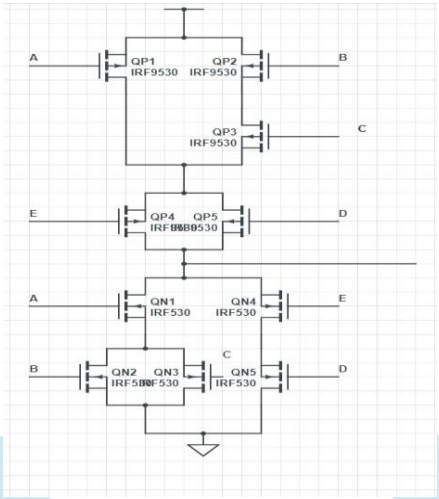
The implementation of CMOS inverters, whether as an amplifier or as a power delay product using VHDL, continues to be a topic of study. It has been claimed that several CAD tools have been used for CMOS logic implementation at various levels. It has been stated that LTSpice can be used to implement memristors. It is crucial to confirm the CMOS inverter's switching characteristics and operating principle since it is one of the key building blocks of static CMOS logic implementation. Circuit level implementation has been used to illustrate power usage in CMOS inverters.

III. PROPOSED DESIGN

The following Boolean equation,
Y=A(B+C)+ED,
has been taken into consideration in this work. Its implementation uses simple AND/OR gates and uses (A, B, C, and D) as its four inputs. Two AND gates and two OR gates are utilised in this Boolean statement. As we are aware, the action of these two gates is AND gate for multiplication and OR gate for addition.

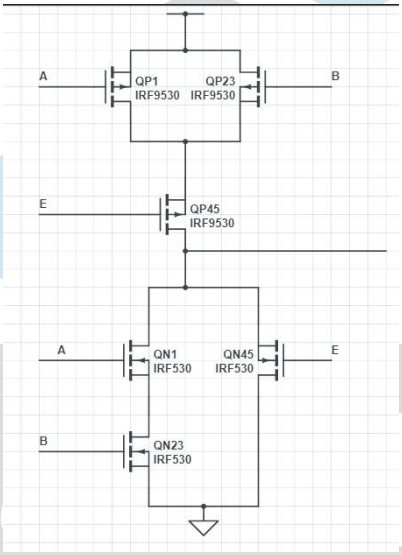


[Fig.(1) RTL Schematic]



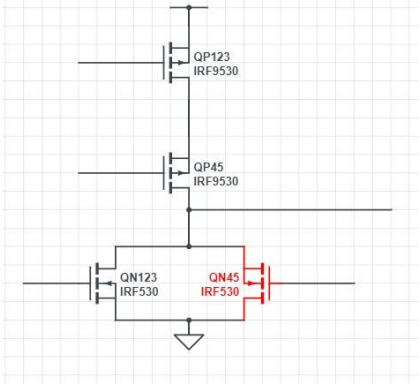
[Fig. (2)(a)CMOS transistor circuit]

The above figure(2)(a) shows the CMOS transistor circuit of the given Boolean expression. In this figure there are used five PMOS and five NMOS. In P-net QP2 and QP3 are in series and QP4 and QP5 are in parallel and in N-net QN2 and QN3 are in parallel and QN4 and QN5 are in series. With the help of transistor equivalency condition QP2 and QP3 are series , so they can be represent as (w/l)of QP23 and QP4 and QP5 are in parallel so they can be represent are (w/l) of QP45 . In this way QN23 is represent for QN2 and QN3 because they both are in parallel and QN45 is represent for QN4 and QN5 because they both are in series which is shown in figure(2)(b).



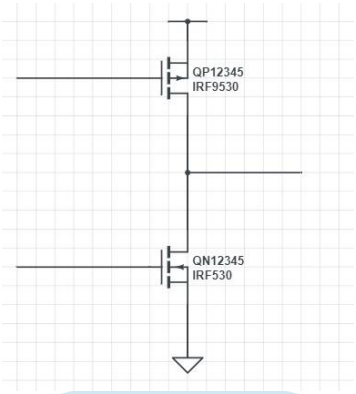
[Fig.(2)(b)]

In the above figure shows that in P-net QP1 and QP23 are in parallel ,so they can be represent as QP123 and in N-net QN1 and QN23 are in series so they can be represent as QN123 which is shown in figure (2)(b).



[Fig.(2)(c)]

In the above figure(2)(c) shows that in P-net QP123 and QP45 are in series ,so they can be represent as (w/l) of QP12345 and in N-net QN123 and QN45 are in parallel so they can be represent as (w/l) of QN12345 which is shown in the fig(2)(d).



[Fig.(2)(d)]

With the help of this transistor equivalency condition we can reduce the N-net and P-net to an equivalent transistor and we get a CMOS inverter circuit from large CMOS transistor circuit. From this inverter we can get our critical voltage values very easily. They are described as follows :

• Output High Voltage, VOH
- maximum output voltage which occurs when input is low (Vin = 0V) • pMOS is ON, nMOS is OFF.The pMOS pulls Vout to VDD–VOH= VDD

• Output Low Voltage, VOL
- minimum output voltage which occurs when input is high (Vin= VDD). Here pMOS is OFF, nMOS is ON and nMOS pulls Vout to Ground–VOL=0v

• Input Low Voltage, VIL – Vin such that
Vin < VIL

$$VIL = \frac{2Vout + VTO(p) - VDD + kR.VTO(n)}{1+kR} \quad (1)$$

• Input High Voltage, VIH – Vin such that
Vin > VIH

$$VIH \frac{= VDD + VTO(p) + kR(2Vout + VTO(n))}{1+kR} \quad (2)$$

$$Vth = \frac{VDD + VTO(p) + \sqrt{kR(VTO(n))}}{1+\sqrt{kR}} \quad (3)$$

• The Noise Margins which represent the tolerance to the circuit to external perturbations which measure of how stable inputs are with respect to signal interference
- NM (H) = VOH - VIH = VDD - VIH
- NM (L) = VIL - VOL = VIL

We must desire our circuit for desirous large NM(H) and NM(L) for best noise immunity.

IV. RESULTS AND DISCUSSIONS

We first implemented the Boolean expression in gate level using Vivado software. The RTL schematic and simulation results have been presented in fig(3) and fig(4) at the point of the cursor at 418.667ns it is observed that

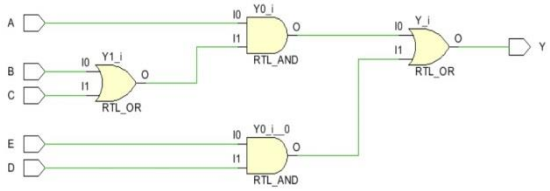


Fig (3) RTL schematic

Fig (4) Simulation result

In Fig(4) shows that, the output Y will be "1," which indicates that the voltage will be "HIGH," when A= "1," B= "0," C= "1," D= "0," and E= "1." We will receive our other output in the same way.

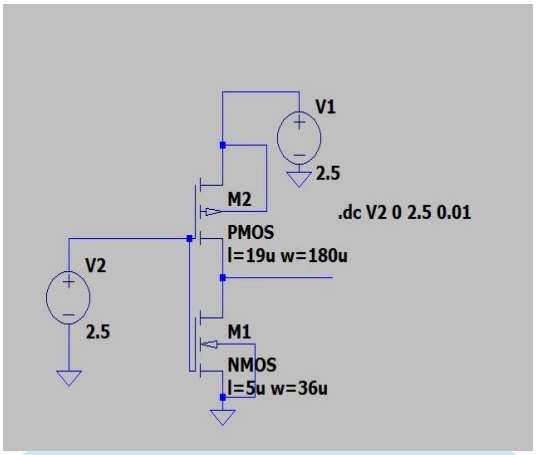


Fig (5) LTSPICE implementation of the reduced circuit

In figure (5) shows that it consists of a enhancement type nMOS and enhancement type pMOS, operating in complementary mode, with input voltage applied to the gate terminal of both the transistor. For high input the nMOS transistor acts as driver which pulls down the output node while the pMOS transistor acts as load. For low input the pMOS transistor acts as driver which pulls up the output node while the nMOS transistor acts as load.

From the circuit w/l of pMOS is 180 µm/19 µm and w/l of nMOS is 36 µm/5 µm. Considering supply voltage V_{DD} = 2.5v, electron mobility, $\mu_n = \frac{110\ cm^2}{V_s}$,hole mobility $\mu_p = \frac{70\ cm^2}{V_s}$ and gate oxide thickness tox= 15nm and the oxide capacitance is

$$\text{Cox} = \frac{Eox}{tox} = \frac{3.97*8.85*10^{-19}}{15*10^{-9}}$$

$$= 2.34 * 10^{-10}\ \text{F/cm}$$

The trans conductance factor (kr) is calculated as

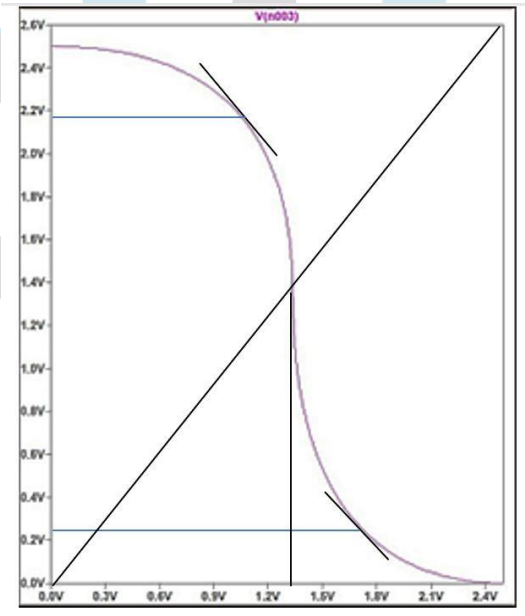
$$\text{kr} = \frac{\mu n\ \text{Cox}\frac{w}{l}n}{\mu p\ \text{Cox}\frac{w}{l}p} = 2.06$$

We know for the CMOS inverter VOH= 2.5V, VOL= 0V.The other critical voltages are calculated from Equations (1) to (3) Vth =1.06V, VIL = 0.65V , VIH = 0.91V. The ΔVth = 0.19V

Finally, we find the noise margins for low voltage levels and for high voltage levels

$$NML = VIL - VOL = 0.91V$$

$$NMH = VOH - VIH = 1.11V$$



[fig.(h) Voltage transfer characteristics of CMOS inverter]

Critical voltages	Simulated values	Calculated values	% of error
VIL	0.31v	0.91v	65%
VIH	2.19v	1.39v	36%
Vth	1.25v	1.06v	18%

The Power analysis from Implemented netlist and the Activity derived from constraints files, simulation files, or vector less analysis shows that the total On-Chip Power is 0.452W, Junction Temperature is 25.9 degrees C, the Thermal Margin is observed to be 59.1 degrees C (31.2W) and no power was. supplied to the off-chip devices. Table I presents the static and dynamic supply details.

Power Supply

Supply Source	Voltage (V)	Total (A)	Dynamic (A)	Static (A)
Vccint	1.000	0.062	0.040	0.022
Vccaux	1.800	0.039	0.027	0.012
Vcco33	3.300	0.000	0.000	0.000
Vcco25	2.500	0.000	0.000	0.000
Vcco18	1.800	0.157	0.156	0.001
Vcco15	1.500	0.000	0.000	0.000
Vcco135	1.350	0.000	0.000	0.000
Vcco12	1.200	0.000	0.000	0.000
Vccaux_io	1.800	0.000	0.000	0.000
Vccbram	1.000	0.000	0.000	0.000
MGTAVcc	1.000	0.000	0.000	0.000
MGTAVtt	1.200	0.000	0.000	0.000
MGTVccaux	1.800	0.000	0.000	0.000
Vccadc	1.800	0.020	0.000	0.020

[Table I Static and Dynamic Power supply parameters]

Power in static $(Pdc) = Vdd * IDC$

IDC = ½[Vin =VOL,Vout = VOH] +[Vin =VOH, Vout = VOL]

= 1/2 [IDn + IDp]

= 0

So $Pdc = Vdd * 0$

$= 0$

From theoretically we get 0A power in static method.

Percentage of error of $Pdc = 2.2\%$

Power in dynamic (Pdy) = $Cl * Vdd^2 * f$

$= 2.34 * 10^{-3} * 9.47 * 1.6$

= 0.03A

So percentage of error = 1%

V. CONCLUSION

In a computer, a logic circuit carries out processing or regulating operations. Information processing is done by this circuit using logical operations. The Boolean values true and false, or 1 and 0, respectively, are represented in logic circuits by two values for a particular physical quantity (voltage, for example). Inputs and outputs that may be reliant on inputs both exist in logic circuits. An arrowhead is shown at the input end of a logic circuit diagram to indicate the link between an output and an input of one circuit.Logic circuits and functions from programming languages are comparable in performance. The inputs resemble function parameters, whereas the outputs resemble the returned values from the function. There can be several outputs supported by a logic circuit.

VI. REFERENCES

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