Double Gate Junction Underlap Dual Gate FinFET for RF and Analog Applications

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Abstract. This paper delves into short channel effects (SCEs) in a double gate (DG) n-FinFET structure, assessing factors like source/drain gate length, oxide variations, and underlap configurations. Introducing underlap concepts showcases enhanced FinFETs performance, a breakthrough for nanoscale applications. These underlap configurations—Drain Underlap (DUL), Source Underlap (SUL), Both Source and Drain Underlap (BUL), and No Underlap (NUL)—represent innovative approaches to mitigate short channel effects, improving control over the channel and reducing leakage. The utilization of a double gate in FinFETs signifies precise control at a nanoscale level. By evaluating these configurations, the research provides insights crucial for advancing semiconductor technology, promising optimized performance, reduced power consumption, and heightened integration density in microchips. Ultimately, this work draws attention to novel strategies for improving transistor behavior and highlights the potential of double-gate FinFETs to push the boundaries of nanoscale applications within semiconductor devices. The reported short-channel effect parameters, notably a DIBL of 182mV/V, SS of 74.4mV/dec, and an Ion/Ioff ratio of 106, portray a highly promising scenario for RF analog applications.

Keywords: FinFETs · SCEs · underlap · no underlap channel · double-gate · work-function.

1 Introduction

The relentless drive toward smaller CMOS technology has been instrumental in achieving higher transistor density and performance. However, as device dimensions shrink towards the nanometer (nm) scale, the conventional single-gate MOSFETs encounter significant hurdles in the form of short-channel effects (SCEs). These effects degrade the current flow (drive current) and contribute to off-state leakage, prompting a quest for innovative solutions in device design and material exploration. One significant stride in overcoming SCEs has been

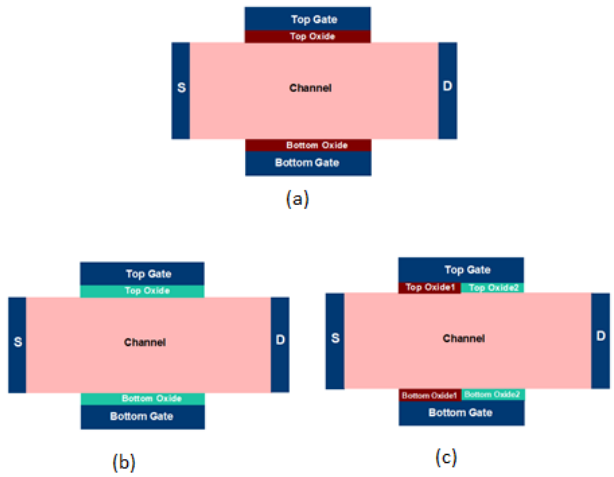

Fig. 1. (a) Double gate n-FInFET structure (Source(S)=Drain(D)=Al), Channel = GaAs, Lsg=Ldg=10nm, tox1=tox2= 2nm= SiO2, Lg-40 nm, (b) Double gate n-FInFET structure (Source(S)=Drain(D)=Al), Channel = GaAs, Lsg=Ldg=10nm, tox1=tox2= 2nm= HfO2, Lg-40 nm (c) Double gate n-FInFET structure (Source(S)=Drain(D)=Al), Channel = GaAs, Lsg=Ldg=10nm, Lox1=20nm-Lox2, Lg-40 nm)

the exploration of alternative structures and materials. Multiple-gate Field Effect Transistors (MuGFETs) have emerged as promising replacements for traditional single-gate planar devices, while FinFETs represent a practical realization of multiple-gate MOSFETs [1–5].

FinFETs, in particular, have demonstrated considerable potential in addressing SCEs while aligning with the downsizing trajectory outlined by the International Technology Roadmap for Semiconductors (ITRS) [2]. Experimental endeavors have showcased the effectiveness of FinFETs in combating SCEs. For instance, a self-aligned double-gate structure scalable to a 20 nm gate length exhibited the ability to suppress SCEs even at a 17 nm gate length [6]. Furthermore, a double-gate FinFET with a gate length as small as 10 nm was successfully fabricated, demonstrating scalability and potential performance enhancements [6-7]. However, despite these advancements, practical constraints loom over further scaling of the FinFET structure. Gate leakage, parasitic resistance and capacitance drain-induced barrier lowering (DIBL), subthreshold swing (SS), and threshold voltage roll-off pose formidable challenges in pushing the limits of FinFET scaling. FinFETs enhance analog/radio-frequency (RF) performance by reducing SS and DIBL[8-12]. However, heavy doping in the channel decreases electron mobility, impacting transistor speed. Engineers seek a balance between improved electrostatics and maintaining acceptable carrier mobility for optimal performance in diverse applications. These constraints necessitate innovative strategies to circumvent or mitigate their impact. An avenue for potential breakthroughs lies in exploring novel channel materials. Group III-V compound semiconductors have emerged as compelling contenders due to their inherent higher electron mobility compared to conventional silicon [9]. These materials offer the promise of sustaining or even enhancing device performance while simultaneously scaling down and operating at a lower supply voltage. This pursuit of alternative materials and device architectures is a collaborative effort between industry and academia. It's a concerted drive to sustain the trajectory set by Moore's Law and the ITRS roadmap, ensuring continued advancements in transistor speed and performance [2].

As researchers delve deeper into material science and device engineering, the potential for innovations in CMOS technology remains vibrant, promising a future of continued progress in semiconductor technology. The paper's subsequent sections detail the device structures, simulation tools employed, various simulation results, analysis of SCEs concerning device scaling parameters, and a conclusion based on the analysis. Subsequent paragraphs, however, are indented.

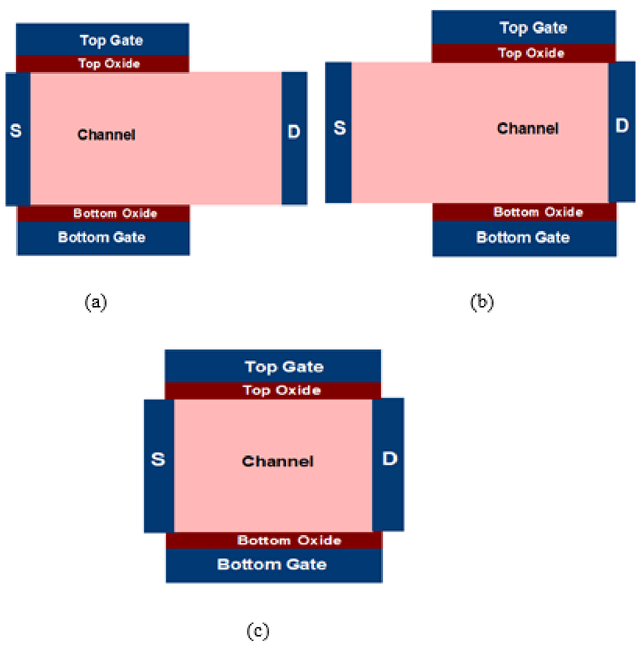

Fig. 2. Double gate n-FinFET (a) 5nm Source underlap (b) 5nm drain underlap (c) Drain=Source-5nm both underlap

2 Device Structure and Simulation Setup

Cogenda's Genius 3D visual TCAD device simulator is being used in order to generate the proposed double-gate n-channel FinFET structure. The three-dimensional (3D) structural view of double-gate FinEFT is shown in the figure. The double-gate n-channel FinFET structure plays a pivotal role in modern semiconductor technology, offering enhanced control over device characteristics compared to traditional planar designs. This structure incorporates various parameters essential for performance analysis. The gate length (Lg =40nm) and channel width (Wth=ranging from 20nm to 40nm) define critical dimensions affecting the transistor's behavior. By varying these dimensions within the specified ranges, engineers gain insights into how the device operates at different scales. A gate length typically enhances switching speed and enables more precise control over the transistor, while the channel width influences current carrying capacity and overall device performance. The oxide thickness (tox1 and tox2) remains consistent at 2nm surrounding the fin, which plays a crucial role in electrostatic control and gate modulation. Consistent oxide thickness ensures uniformity in electrical characteristics across the channel, impacting parameters like leakage current and gate capacitance. Doping levels, such as fixed drain/source doping and channel doping, determine carrier concentrations within the channel. These concentrations significantly affect the device's conductivity and threshold voltage (V_{th}).

Here in this paper, the used channels with work functions are the P-channel (work function ϕ(f) =4.65) and for the N-channel (work function ϕ(f)=4.82eV). The simulation is accomplished here at physical model of fermi-Dirac carrier statics and the material model of Hypertang mobility for channel (GaAs) are used for simulating nanoscale devices. Making the underlap region lightly doped lead to reduction in leakage current but Ion degrades due to enhancement in source/drain resistance [1]. The varying gate bias allows examination of the transistor's response to different gate potential, crucial for assessing its switching behavior and power consumption. Simulation studies encompassing these parameter variations provide a comprehensive understanding of the device's electrical characteristics, including threshold voltage, transconductance, and subthreshold behavior. Engineers leverage such simulations to optimize the FinFETs performance for specific applications, balancing factors like speed, power consumption, and reliability. Understanding how these parameters interplay within the FinFET structure aids in designing transistors tailored for diverse applications,spanning from high-performance computing to low-power portable devices, ultimately driving advancements in semiconductor technology.

3 Results and Discussions

The device structure is simulated in TCAD software and different parameters are analyzied as below.

3.1 Drain current versus Gate Voltage for different oxide layer

In order to study the input characteristics (I_{ds} vs. V_{gs}) at constant V_{ds}, the n-FinFET structure has been simulated with various oxide thicknesses (t_{ox1} and t_{ox2}) for Silicon dioxide (SiO2)=2nm, Hafnium(IV) oxide (HfO2)=2nm and SiO2-HfO2 (SiO2=1nm= HfO2) For a fixed channel length (Lg) of 40nm and a work function(f) of 4.82. from the characteristics obtained, it has been observed that For FinFETs utilizing these different oxide layers, the Ids vs. Vgs curves can show variations in threshold voltage, subthreshold slope, and leakage current characteristics. HfO2-based FinFETs generally tend to exhibit better performance in terms of leakage reduction and improved gate control helps achieve higher ON-state currents and better transistor performance.

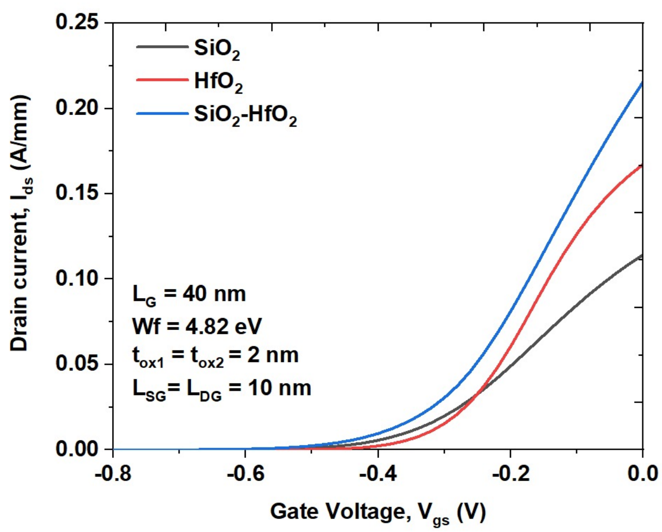

Fig. 3. Input characteristics (I_{ds} vs. V_{gs}) at constant Vds

3.2 Transconductance versus Gate Voltage for different oxide layer

From the result shown in Fig. 4, it is clear that for a channel length (Lg) of 40nm, n-FinFET has been simulated with transconductance (gm) of a transistor represents its ability to amplify signals, measured as the change in drain current (Id) with respect to the change in gate voltage (Vg). For FinFETs with different oxide layers like SiO2 and HfO2, the transconductance versus gate voltage curves can exhibit distinct behaviors due to variations in gate dielectric properties.The transconductance(gm) curve for HfO2-based n-FinFET shows a sharper increase in transconductance with gate voltage due to improved gate controllability.

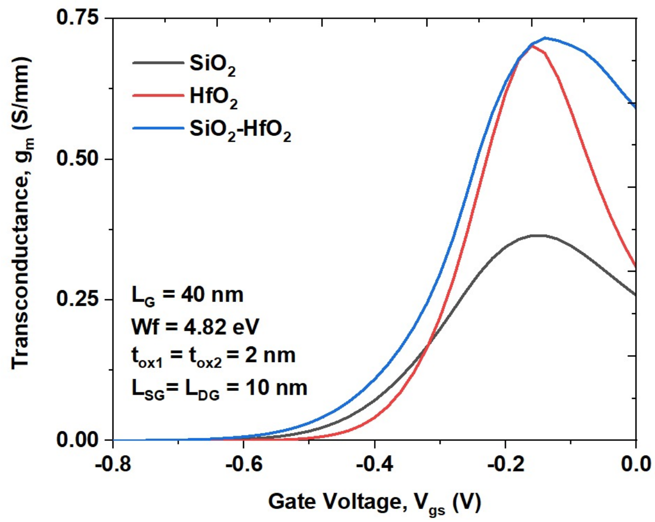

Fig. 4. Transconductance Curve for different oxide layers

3.3 Drain current versus gate voltage for different underlap source-drain

The transfer characteristics of the simulated Double-Gate (DG) n-FinFET for GaAs channel for Lg=40nm, f= 4.82eV and various source-drain underlap regions i.e.,DUL-drain underlap (Ldg=15nm,Lsg=10nm), SUL- source underlap (Lsg=15nm,Ldg=10nm), BUL- both source and drain underlap (Ldg=Lsg=15nm) and NUL- no underlap (Ldg=Lsg=10nm) respectively is shown in fig. 5. It is found that at SUL and DUL shows comparatively similar results. Overall, the combining underlap source-drain with the gate voltage modulation allows for optimizing transistor behavior for specific applications, achieving better performance and power efficiency in modern semiconductor devices, especially FinFETs.

3.4 Drain current versus gate voltage for different Length of drain/source gate

In fig.6, simulation results of Drain current (Ids) variation with length of source-gate (Lsg) and length of drain-gate (Ldg) have been presented, wherein the gate length (LG) and oxide thickness (tox1=tox2) has been kept constant at 40nm and 2nm respectively. For this study the Ldg and Lsg has been varied over 5 to 10 nm, and the devices were again simulated individually for each variation. From the characteristics obtained, it has been observed that the specific impact of drain/source to gate lengths on the drain current versus gate voltage characteristics depends on various factors, including fabrication processes, doping

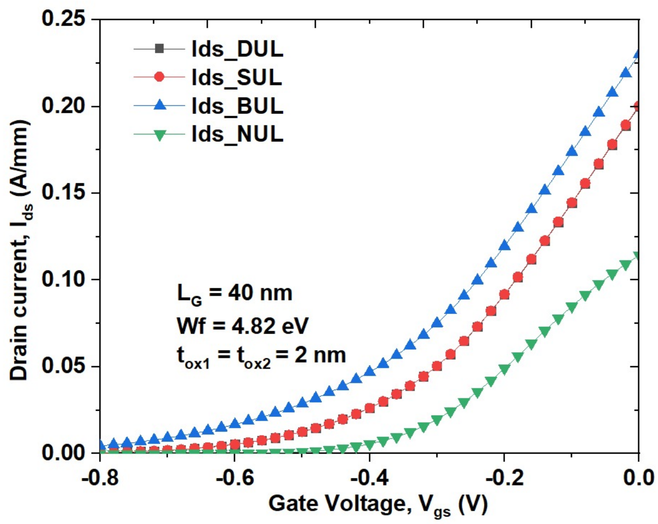

Fig. 5. Drain current versus gate voltage for different underlap conditions

profiles, and the overall transistor geometry. Additionally, while shorter lengths generally contribute to higher performance, they may also pose challenges in terms of manufacturing precision and controlling short-channel effects.

3.5 Transconductance versus gate voltage and Length of drain/source gate

The transconductance curve of the Double-Gate (DG) n-FinFET for GaAs channel for Lg=40nm, f= 4.82eV and oxide thickness (tox1=tox2) =2nm. In this study, variations in drain-to-gate (Ldg) and source-to-gate (Lsg) lengths from 5 to 10 nm were individually simulated for each parameter. The investigation aimed to understand their impact on transistor performance, considering factors such as channel resistance, gate control, and signal amplification in the devices under study. From the result shown in fig. 7, it is clear that Transconductance (gm) typically increases with gate voltage for a given drain/source to gate length, showcasing the transistor's ability to amplify signals at higher gate voltages. For transistors with shorter drain/source to gate lengths, the transconductance versus gate voltage curve exhibit sharper increases in transconductance (gm) with increasing gate voltage due to improved gate control over the channel.

3.6 Transconductance versus gate voltage and underlap source-drain

The transconductance (gm) versus gate voltage (Vg) curve for the simulated Double-Gate (DG) n-FinFET with a GaAs channel, considering different source-

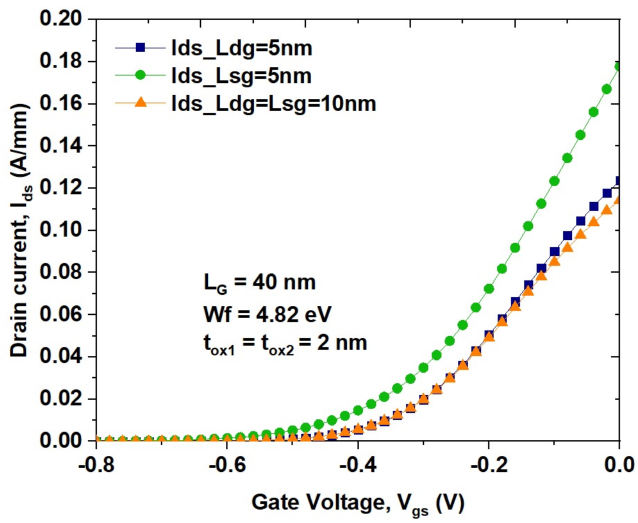

Fig. 6. Drain current versus gate voltage for different Length of drain/source gate

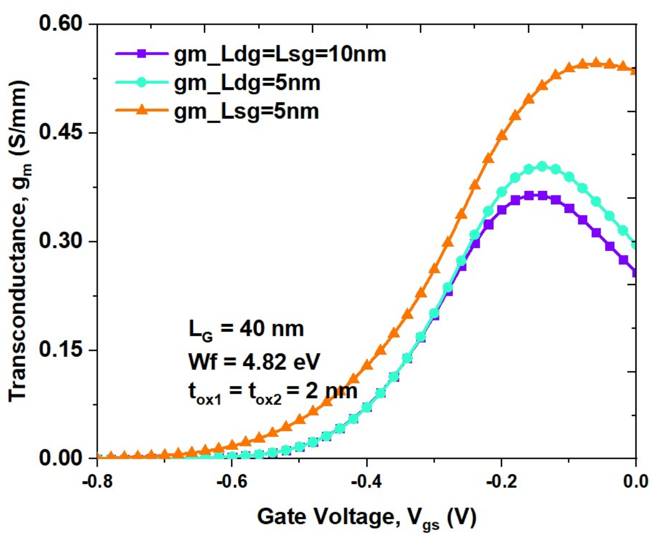

Fig. 7. Transconductance versus gate voltage for different Length of drain/source gate

drain underlap configurations: DUL (Drain Underlap): Ldg=15nm, Lsg=10nm,SUL (Source Underlap): Lsg=15nm, Ldg=10nm,BUL (Both ,Source and Drain Underlap): Ldg=Lsg=15nm and NUL (No Underlap): Ldg=Lsg=10nm is shown in fig.8.These simulations aimed to examine how transconductance varies concerning gate voltage for specific configurations of source-drain underlap regions, maintaining a gate length (Lg) of 40nm and work function ϕ(f) of 4.82eV for the GaAs channel. This analysis provides insights into the amplification capabilities and control of the transistor under different underlap conditions, critical for optimizing transistor performance in various operating scenarios.

In order to study the transconductance (gm) against gate voltage (Vg) curve in transistors is influenced by underlap source-drain configurations. Varying underlap lengths alongside gate voltage alters the gm vs. Vg curve. Underlap minimizes leakage, enhances control, and, when coupled with gate modulation, optimizes amplification capabilities. This synergy refines transistor behavior for improved performance across different operating conditions.

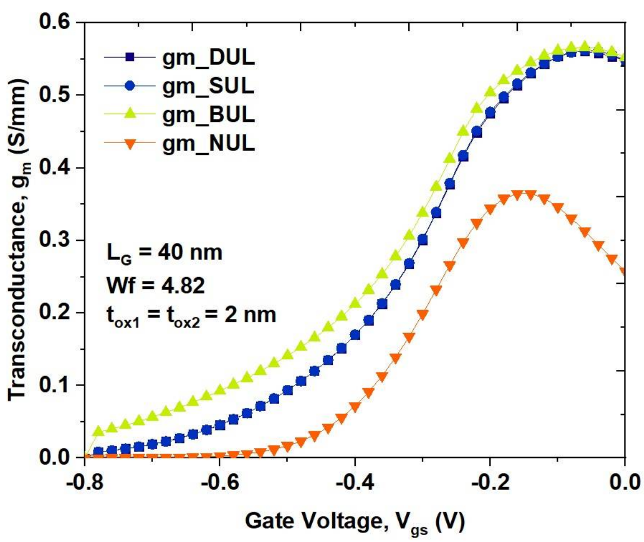

Fig. 8. Transconductance versus gate voltage for different underlap conditions

3.7 Drain current versus Drain voltage relationship in different n-FinFET devices

There are a number of things that can change the output characteristics curve (at constant Vgs) in different nFinFET devices. These include the length of the source/drain gate, the oxide variation (SiO2 and HfO2), and the underlap configurations (DUL, SUL, BUL, NUL). This relationship is crucial to understanding the device's behavior under different operating conditions. Length of Source/Drain to Gate (Lsg, Ldg): altering these lengths impacts the output characteristics, affecting drain current behavior concerning drain-source voltage. Different gate dielectrics (e.g., SiO2 and HfO2) have distinct electrical properties affecting the output curve. Varying source-drain underlap configurations can significantly affect the drain current behavior at different drain-source voltages. Underlap changes leakage currents, threshold voltage, and subthreshold behavior, influencing the output characteristics curve.

Analyzing the output characteristics at constant gate-source voltage while manipulating these factors allows for a comprehensive understanding of their individual and combined impacts on device performance. Variations in drain current behavior due to underlap, gate dielectric choice, and source/drain to gate lengths help engineers optimize n-FinFET designs for specific applications, balancing factors such as power efficiency, performance, and reliability under varying operating conditions.

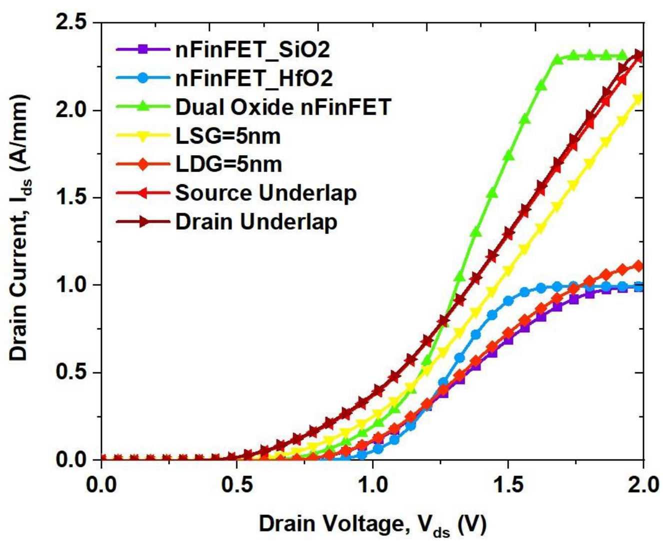

Fig. 9. Drain current versus Drain voltage relationship in different n-FinFET devices

3.8 Drain current versus Drain Voltage relationship in n-FinFET and p-FinFET

The output characteristics curve The relationship between drain current (Id) and drain voltage (Vds) in n-channel and p-channel FinFETs is similar, but the polarities are different because the n-channel has electrons and the p-channel has holes as carriers. The drain current in a FinFET is influenced by several factors, including gate voltage, drain voltage, channel length, width, and doping concentration. The fundamental behavior is dictated by the channel properties, biasing conditions, and nature of charge carriers within the semiconductor channel.

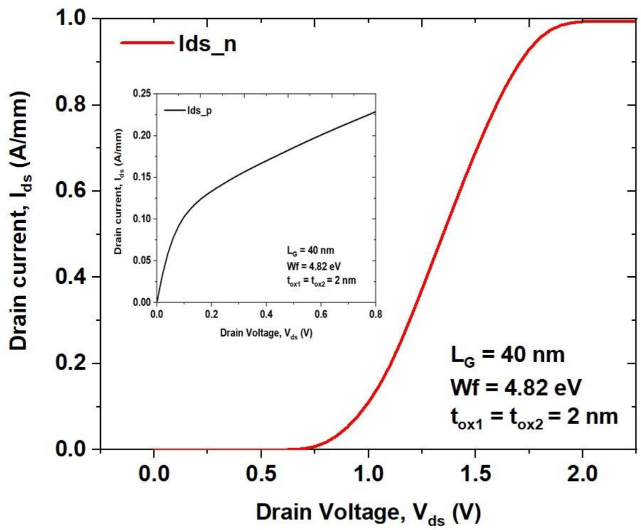

Fig. 10. Drain current versus Drain Voltage relationship in n-FinFET and p-FinFET

Below equations are used to calculate the DIBL and SS parameter.

$$DIBL(mV/V) = \left| \frac{Vt1 - Vt2}{Vds1 - Vds2} \right| \tag{1}$$

$$SS(mV/dec) = \left(\frac{\partial \log_{10} I_{ds}}{\partial V_{gs}} \right)^{-1} \tag{2}$$

4 Conclusions

A comparative study based on short channel effects viz., DIBL (drain-induced barrier lowering), SS (subthreshold swing), and VT (threshold voltage) by conducting several factors, including length of source/drain gate, oxide variation (SiO2 and HfO2), and underlap configurations (DUL, SUL, BUL, NUL) in FinFET structures, aims to provide insights into how different material choices impact short-channel effects. Understanding these effects aids in optimizing transistor designs for improved performance, reduced power consumption, and better reliability as transistors are scaled down, contributing to advancements in

Table 1. Different parameters comparison among various FinFET structures

Devices	Ioff (A/μm)	Ion/Ioff	V_T (V)	DIBL (mV/V)	SS (mV/dec)
P-FinFET	$3.7*10^{-9}$	$0.3*10^{5}$	0.612	198	94
n-FinFET(SiO2)	$3.16*10^{-9}$	$0.36*10^{5}$	0.519	184	81
n-FinFET(HfO2)	$1.03*10^{-10}$	$1.62*10^{4}$	0.412	182	74.4
n-FinFET(SiO2-HfO2)	$1.52*10^{-8}$	$1.42*10^{4}$	0.458	251	84
SUL n-FinFET(5 nm)	$6.95*10^{-7}$	$0.25*10^{3}$	0.609	234	98.6
DUL n-FinFET(5 nm)	$7.06*10^{-7}$	$0.28*10^{3}$	0.602	246	92
BUL n-FinFET(10 nm)	$4.51*10^{-6}$	$0.51*10^{2}$	0.574	190	76.2

semiconductor technology. P-channel FinFET (ϕ(f) = 4.65 eV) is suitable for creating a p-channel transistor. A lower work function implies the semiconductor's ability to attract positive charges (holes) more easily. wherein N-channel FinFET (ϕ(f) = 4.82 eV) corresponds to creating an n-channel transistor. A higher work function implies the semiconductor's propensity to attract negative charges (electrons) more easily. Off-State Characteristics of Both the p-channel and n-channel transistors exhibit an 'off' state where there's minimal to negligible current flow between the drain and source terminals when the gate-source voltage is below the threshold voltage. The reported short-channel effect parameters, notably a DIBL of 182mV/V, SS of 74.4mV/dec, and an Ion/Ioff ratio of 106, portray a highly promising scenario for low-power applications. The BUL n-FinFET configuration exhibits further enhancements, showcasing a DIBL of 190mV/V and an SS of 76.2mV/dec. These results show how important it is for source and drain regions to be overlapping in FinFET structures. This gives you better control over short-channel effects and shows how they can be used to improve device performance in low-power semiconductor applications.

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