ODISHA UNIVERSITY OF TECHNOLOGY AND RESEARCH

Techno Campus, Mahalaxmi Vihar, Ghatikia, Bhubaneswar-751029.

Syllabus (Effective from 2023-24)

School/ Department: School of Electronic Sciences

Course: M. Tech., Programme: VLSI Design and Embedded Systems (VLSI),

Duration: 2 years (Four Semesters)

Abbreviation used:

AC	Audit course	LC	Lab Course	PA	Practical Assessment
PC	Professional Core	PR	Project/ Practical/ Internship	L	Lecture
PE	Professional Elective	SE	Seminar/ Expert Lecture/ Etc.	T	Tutorial
OE	Open Elective	IA*	Internal Assessment	P	Practical
MC	Mandatory/ Common Course	EA	End-Semester Assessment		

Subject Code Format:

A1	A2	B3	C4	C5	C6
School/ Dept. (Offering) **BH:** Basic Sciences and Humanities **CS:** Computer Sciences **EE:** Electrical Sciences **EI:** Electronic Sciences **IP:** Infrastructure and Planning **MS:** Mechanical Sciences **BT:** Biotechnology **TE:** Textile Engineering		**Level** **1:** UG/ Int. Msc. (1st Year) **2:** UG/ Int. Msc. (2nd Year) **3:** UG/ Int. Msc. (3rd Year) **4:** UG/ Int. Msc. (4th Year) **5:** UG/ Int. Msc. (5th Year) **6:** PG (1st Year) **7:** PG (2nd Year) **8:** Ph.D.	**0:** AC **1:** PC **2:** PE **3:** OE **4:** MC **5:** LC **6:** PR **7:** SE **8:** **9:**	**Serial Number (01 to 99)** 01/ 03/…/ 19: Odd Sem. (ECE) 21/ 23/…/ 39: Odd Sem. (ICE) 41/ 43/…/ 59: Odd Sem. (VLSI) 61/ 63/…/ 79: Odd Sem. (Prog-4) 81/ 83/…/ 99: Odd Sem. (Prog-5) 02/ 04/…/ 20: Even Sem. (ECE) 22/ 24/…/ 40: Even Sem. (ICE) 42/ 44/…/ 60: Even Sem. (VLSI) 62/ 64/…/ 80: Even Sem. (Prog-4) 82/ 84/…/ 98: Even Sem. (Prog-5)	

1st Semester

Sl. No.	Subject Type	Subject Code	Subject Name	Teaching Hours			Credit	Maximum Marks			
				L	T	P		IA	EA	PA	Total
1	PC 1	EI6141	Digital VLSI Design	3	0	0	3	40	60	-	100
2	PC 2	EI6143	Analog Integrated Circuit Design	3	0	0	3	40	60	-	100
3	PE 1 (Any One)	EI6241	VLSI Fabrication Techniques	3	0	0	3	40	60	-	100
		EI6243	VLSI Signal Processing								
		EI6245	VLSI CAD								
4	MC 1	BH6401	Mathematical Methods in Engineering	3	0	0	3	40	60	-	100
5	MC 2	MS6403	Research Methodology and IPR	2	0	0	2	40	60	-	100
6	LC 1	EI6541	IC Design Lab	0	0	4	2	-	-	100	100
7	LC 2	EI6543	Design and Simulation Lab	0	0	4	2	-	-	100	100
8	AC 1	Any One from the List of AC 1 (Appendix-I)		2	0	0	0	40	60	-	100
			Total	**16**	**0**	**8**	**18**	**240**	**360**	**200**	**800**

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2nd Semester

Sl. No.	Subject Type	Subject Code	Subject Name	Teaching Hours			Credit	Maximum Marks			
				L	T	P		IA	EA	PA	Total
1	PC 3	EI6142	Embedded System Design	3	0	0	3	40	60	-	100
2	PC 4	EI6144	Modeling and Synthesis with HDL	3	0	0	3	40	60	-	100
3	PE 2 (Any One)	EI6242	VLSI Design Verification and Testing	3	0	0	3	40	60	-	100
		EI6244	Mixed Signal & RF IC Design								
		EI6246	Low Power VLSI System								
4	PE 3 (Any One)	EI6248	Hardware Software Co-design	3	0	0	3	40	60	-	100
		EI6250	Hardware Security								
		EI6252	ASIC and SoC Design								
5	OE 1	Any One from the List of OE 1 (Appendix-I)		3	0	0	3	40	60	-	100
6	PR 1	EI6642	Project (Specialization Related)	0	0	4	2	-	-	100	100
7	LC 3	EI6542	Embedded System and HDL Lab	0	0	4	2	-	-	100	100
8	AC 2	Any One from the List of AC 2 (Appendix-I)		2	0	0	0	40	60	-	100
			Total	**17**	**0**	**8**	**19**	**240**	**360**	**200**	**800**

3rd Semester

Sl. No.	Subject Type	Subject Code	Subject Name	Teaching Hours			Credit	Maximum Marks			
				L	T	P		IA	EA	PA	Total
1	PE 4* (Any One)	EI7241	Semiconductor Device Modeling and Simulation	3	0	0	3	40	60	-	100
		EI7243	Nanomaterials and Nanotechnology								
		EI7245	Micro Electromechanical Systems								
2	PR 2	EI7641	Dissertation (Phase-I)	0	0	24	12	-	-	100	100
			Total	**3**	**0**	**24**	**15**	**40**	**60**	**100**	**200**

* Virtual/Online Course either offered by OUTR or available in MOOCs platform (No physical class)

4th Semester

Sl. No.	Subject Type	Subject Code	Subject Name	Teaching Hours			Credit	Maximum Marks			
				L	T	P		IA	EA	PA	Total
1	PR 3	EI7642	Dissertation (Phase-II)	0	0	32	16	-	-	100	100
			Total	**0**	**0**	**32**	**16**	**-**	**-**	**100**	**100**

Credits and Maximum Marks

Sl. No.	Semester	Credits	Maximum Marks
1	1st	18	800
2	2nd	19	800
3	3rd	15	200
4	4th	16	100
	Total	68	1900

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1st Semester

PC 1	EI6141	Digital VLSI Design	3	0	0	3

Course Outcomes: By the end of the course, students should be able to:

1. Apply the basics of MOS transistor theory to calculate its design and electrical parameters.
2. Analyze a transistor using the concept of scaling theory and short channel effects.
3. Analyze the CMOS inverter for deriving its critical voltages, noise margin, power, rise time, fall time and propagation delay and draw layout and stick diagrams.
4. Perform transistor level implementations of simple digital circuits and memory module using CMOS and other static and dynamic logic and apply transistor equivalency to reduce a static logic design to its inverter equivalent.

Module I

Introduction: Historical Perspective, Issues in IC Design, Design Metrics.
MOS Transistor and Layout: Basic MOSFET Characteristics, Current-Voltage Characteristics, Layout Diagrams.
Short Channel Effects: Scaling Theory, Threshold Voltage Variation, Mobility Degradation, Velocity Saturation, Hot Carrier Effects, Subthreshold Slope, DIBL, GIDL.

Module-II

CMOS Inverter: Introduction to Static CMOS Design, Transfer Curves and Noise Margins, Gate Delays and Rise and Fall Times, Switching Threshold Voltage, Power, Energy, and Energy-Delay, CMOS Inverter Dynamic Behavior, Transistor Equivalency.
CMOS Logic Gates: Pseudo-NMOS Logic, Complementary CMOS, Pass-Transistor Logic, Transmission gates, Differential CMOS Circuits, Dynamic Logic.

Module III

Basic Building Blocks: Logic Gates, Adders, Flip-Flops, CMOS Clocked Latches.
MOS memories: Introduction, DRAM, SRAM, Nonvolatile Memory, Flash Memory.

Text books:

1. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, Digital Integrated Circuits – A Design Perspective, 2nd Edn., Pearson Education, 2003. ISBN: 8178089912.

Reference Books:

2. J. P. Uyemura, Introduction to VLSI Circuits and Systems, Wiley
3. Sung-Mo Kang, Yusuf Leblebici, CMOS Digital Integrated Circuits, TMH, 2014

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PC 2	EI6143	Analog Integrated Circuit Design	3	0	0	3

Course Outcomes: By the end of the course, students should be able to:

1. Understand the basics of analog integrated circuit design and MOS models.
2. Design basic analog integrated circuits.
3. Analyze the performance and limitations of analog integrated circuits.
4. Analyze the effect of noise in MOSFETs.

Module I

Introduction to Analog IC Design, The Design Flow of Analog ICs, MOSFET Parameters, MOSFET models, MOS Diode, MOS Capacitors, MOS Switch.

MOS Current sources and current sink circuits, Voltage and Current reference circuits, MOS Gain stages, Source Followers.

Module-II

Amplifiers, Differential Amplifiers, Operation Amplifiers, Stability Theory and Compensation in CMOS Operational Amplifiers, OPAMP Design Techniques and practical consideration in design of OPAMP, High Performance CMOS OPAMP Design,

Module III

Design of MOS Comparators, Switch Capacitor Filters, Mismatch Issues in Analog Layouts, Noise in MOSFETs.

Text books:

1. B. Razavi, Design of Analog CMOS Integrated Circuits, Tata McGraw-Hill , 2002.
2. Franco Maloberti, Analog Design for CMOS VLSI Systems, Springer New York, NY.

Reference Books:

3. P.E. Allen and D.R.Holberg, CMOS Analog Circuit Design, Oxford University Press , 2004
4. R.J.Baker, H. W. Li, D. E. Boyce, CMOS Circuit Design, Layout, and Simulation, PHI , 2002

PE 1	EI6241	VLSI Fabrication Techniques	3	0	0	3

Course outcomes: At the end of the course, the student will be able to:

1. Get a brief idea about crystal growth and wafer manufacturing in a cleanroom environment.
2. Understand the basic fabrication process steps with lithography, deposition, and ion-implantation.
3. Acquire the concepts of various thin film deposition, metallization and interconnect deposition and analysis for IC fabrication.
4. Importance of Photolithography, Etching, Diffusion, Ion implantation.

MODULE – I

Introduction: Semiconductor materials and Integrated Circuit Fabrication.

Overview of IC Technology: Types of Integrated Circuits, Advantages, and disadvantages of Integrated Circuits.

Crystals: Moore's Law and material processing, Defects in crystals, Czochralski (CZ) and the Floating Zone (FZ) methods of making silicon wafers, Different wafer orientation.

Fabrication steps: Epitaxial growth, Oxidation for isolation, Lithography and Lithographic Technologies, Photolithography, Etching, Diffusion, Ion implantation, Metallization, Process Integration in IC Fabrication, Testing for reliability, Packaging protection, IC Packaging and Testing**.**

Clean Rooms: Clean Room Classifications, comparison between selected equivalent of FS 209E (FED STD-209E) and ISO 14644-1.

MODULE – II

Fabrication steps for different circuits: Resistors, capacitors, transistor. Ohomic contact and Schottky contact, Schottky Diode.

Epitaxial Silicon Deposition: Definition, Purposes, Epitaxy Reactors, Epitaxy Process, Vapour phase epitaxy, LPE, MBE, CVD deposition of Polysilicon.

Diffusion: Constant & limited source diffusion, Concentration dependent diffusion, Field assisted diffusion, Junction depth, Open tube and closed tube diffusion, Diffusion sources.

Ion Implantation: Basic process, Ion Implantation Systems, Ion penetration and profile, Ion Implantation Damage, Annealing.

MODULE – III

Oxidation: Purpose, Dry and wet oxidation, Deal-Grove model, Oxidation system, Properties of oxides – Masking and charges in oxides Deposition Processes.

Lithography: Negative vs Positive photoresist, Mask Alignment and UV Exposure (Contact printing, Proximity printing, Projection printing), Electron beam and X-ray lithographic techniques. Processing Sequence in Photolithography, Problems in lithography.

Etching: Wet Etching, Isotropic and Anisotropic Etching, Plasma Etching, Reactive Ion Beam Etching.

IC Process Integration: Bipolar Transistor Fabrication, Isolation techniques, P-MOS, N-MOS and C-MOS processes.

Text Books:

1. S.K. Gandhi, VLSI Fabrication Principles: Silicon and Gallium Arsenide, Wiley India Pvt. Ltd., New Delhi, 2nd edn. (1994), ISBN: 0471580058.
2. Marc J. Madou, Fundamentals of Micro fabrication, CRC Press (2002), ISBN: 0849308267

Reference Books:

1. J. Plummer, M. Deal and P. Griffin, Silicon VLSI Technology, Prentice Hall, 2000, ISBN:0130850373.
2. S.M.Sze, VLSI Technology, Tata McGraw Hill, 1983, ISBN: 0070582912.

PE 1	EI6243	VLSI Signal Processing	3	0	0	3

Course Outcome:

1. Understand VLSI design methodology for signal processing systems.
2. Be familiar with VLSI algorithms and architectures for DSP.
3. Be able to implement basic architectures for DSP using CAD tools.

MODULE-I

Pipelining and Parallel Processing: Introduction, Pipelining of FIR Digital Filters, Parallel Processing. Pipelining and Parallel Processing for Low Power. Retiming: Introduction, Definition and Properties, Solving System of Inequalities, Retiming Techniques.

MODULE-II

Unfolding: Introduction an Algorithms for Unfolding, Properties of Unfolding, Critical Path, Unfolding and Retiming Application of Unfolding. Folding: Introduction to Folding Transformation, Register Minimization Techniques, Register Minimization in Folded Architectures, Folding in Multi-rate Systems.

MODULE-III

Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations Containing Delays.

Fast Convolution: Introduction, Cook, Toom Algorithm, Winograd Algorithm, Iterated Convolution, Cyclic Convolution, Design of Fast Convolution Algorithm by Inspection.

Text Books:

1. Keshab K. Parhi. VLSI Digital Signal Processing Systems, Wiley-Inter Sciences, 1999
2. Mohammed Ismail, Terri, Fiez, Analog VLSI Signal and Information Processing, McGraw Hill, 1994.
3. Kung. S.Y., H.J. While house T. Kailath, VLSI and Modern signal processing, Prentice Hall, 1985.
4. Jose E. France, Yannis Tsividls, Design of Analog Digital VLSI Circuits for Telecommunications and Signal Processing' Prentice Hall, 1994.

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PE 1	EI6245	VLSI CAD	3	0	0	3

Course Outcomes: At the end of the course the student will be able to:

1. Specify layout techniques in IC.
2. Identify algorithms required for circuit simulators.
3. Incorporate timing analysis and floor planning.
4. Apply scripting language PERL to improve EDA tool flow.
5. Specify layout techniques in IC.

Module I

Introduction to Design Methodologies: The VLSI Design Problem, Design Methods and Technologies, Layout Methodologies, Top-Down Approach: Routing: Fundamentals, Global Routing, Detailed Routing.

Module II

Performance Issues in Circuit Layout: Delay Models, Timing Driven Placement, Timing Driven Routing, Power Minimization.

Single-Layer Routing and Applications: Planar Subset Problem, Single-Layer Global Routing, Over-the-cell Routing, Multichip Modules, Wire-Length and Bend Minimization Techniques.

Module III

Cell Generation and Programmable Structures: Programmable Logic Arrays, Transistor Chaining, Weinberger Arrays and Gate Matrix Layout, CMOS Cell Layout Styles Considering Performance Issues, Compaction: 1D Compaction, 2D Compaction.

Text Books:

1. S.H. Gerez, Algorithms for VLSI Design Automation, Wiley, 2006.
2. M. Sarrafzadeh and C. K. Wong, An Introduction to VLSI Physical Design, McGraw Hill, 1996.

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MC 1	BH6401	Mathematical Methods in Engineering	3	0	0	3

Refer Appendix-I for detailed Syllabus.

MC 2	MS6403	Research Methodology and IPR	2	0	0	2

Refer Appendix-I for detailed Syllabus.

LC 1	EI6541	IC Design Lab	0	0	4	2

Course Outcomes:

The students will be able to

1. Gain basic knowledge as well as hands on experience on CMOS inverter.
2. Design complex logic circuits.
3. Familiarize and implement pass transistor logic.

Circuit design and Layout using Micro wind/ Symica/ SPICE tools/ Cadence
(At least 2 experiments from each)

1. nMOS Inverters and circuits
2. CMOS Inverters and circuits.
3. Transmission gate: Switch, MUX
4. Pass Transistor Logic
5. CMOS Analog Circuits

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LC 2	EI6543	Design and Simulation Lab	0	0	4	2

Course Objectives:

The students will be able to

1. Develop circuit level modeling on primitive semiconductor devices such as diode, transistor, MOSFET and advanced device.
2. Design CMOS based circuits.
3. Design heterojunctions.

Simulation of the following semiconductor devices using CAD tools and Modeling **using MATLAB**

- PN Junction
- MOS Transistor
- CMOS Inverter
- Advanced devices (At least 2) (Egs. Heterojunction, TFET, FinFET etc.)

AC 1	Any One from the List of AC 1 (Appendix-I)	2	0	0	0

Refer Appendix-I for detailed Syllabus.

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2nd Semester

PC 3	EI6142	Embedded System Design	3	0	0	3

Prerequisite:

- Familiarity with microcontrollers/microprocessors
- Basic coding skills

Course Outcomes:

1. Understand the concept of embedded systems, including their characteristics and applications, challenges.
2. Apply common design metrics to evaluate the performance and quality of embedded systems and Utilize specification techniques to describe an embedded system behavior.
3. Apply the understanding of ARM to embedded system design and create and execute sample programs using ARM assembly language instructions.
4. Understand various communication protocols and task scheduling algorithms commonly used in embedded systems.

Module I

Introduction to Embedded Systems: Embedded systems Overview, Characteristics of embedded computing applications. Design Challenges, Common Design Metrics, Embedded systems Design flow.

Specification Techniques: State charts, Specification Description Language (SDL), Petri Nets, Unified Modeling Language (UML).

Module II

Introduction to ARM Processors:

Background of ARM and ARM Architecture, ARM Pipeline

ARM Cortex programming:

Assembly basics, Instruction set, Data transfer, Data processing, conditional and branch instructions, Thumb2 instructions, Sample data transfer, arithmetic and logical assembly language programs.

Module III

Embedded Systems Interfacing:

Serial Peripheral Interface (SPI), Inter Integrated Circuit (I2C), RS-232, Universal Serial Bus (USB), CAN, IrDA, Bluetooth, PCI and AMBA bus protocols.

RTOS and Scheduling

RTOS and its requirements, Task Scheduling, Scheduling Algorithms- Clock Driven and Event Driven Algorithms

Text Books:

1. Joseph Yiu, The Definitive Guide to ARM Cortex-M3 and Cortex-M4 Processors, Newnes Publications; 3rd edition, 2013.
2. Peter Marwedel, Embedded System Design, Springer, ISBN 978-3-319-56043-4
3. Santanu Chattopadhya, ―Embedded System Design‖, PHI, 2nd Edition.
4. Frank Vahid and Tony Givargis, ―Embedded System Design‖, John Wiley & sons Inc.3rd Edition.

Reference Books:

1. Raj Kamal, Embedded Systems- Architecture, Programming and Design, 3rd Edition, 2017.
2. Lyla B. Das, Architecture, Programming, and Interfacing of Low-power processors- ARM7, Cortex, 2017, Cengage, ISBN 978-81-315-3401-4

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PC 4	EI6144	Modeling and Synthesis with HDL	3	0	0	3

Course Outcomes:

At the end of this course, students will be able to

CO1: Write Verilog programs in gate, dataflow (RTL), behavioral and switch modeling levels of Abstraction.
CO2: Design and verify the functionality of digital circuit/system using test benches.
CO3: Identify the suitable Abstraction level for a particular digital design.
CO4: Write the programs more effectively using Verilog/VHDL

Module I

Overview of Digital Design with HDL: Evolution of CAD, emergence of HDLs, typical HDL-flow.
Hierarchical Modeling Concepts: Top-down and bottom-up design methodology, differences between modules and module instances, parts of a simulation, design block, stimulus block.
Basic Concepts: Lexical conventions, datatypes, system tasks, compiler directives.

Module II

Modules and Ports: Module definition, port declaration, connecting ports, hierarchical name referencing.
Gate-Level Modeling: Modeling using basic HDL gate primitives, description of and/or and buf/not type gates, rise, fall and turn-off delays, min, max, and typical delays.
Dataflow Modeling: Continuous assignments, delay specification, expressions, operators, operands, operator types.

Module III

Behavioral Modeling: Structured procedures, initial and always, blocking, and non- blocking statements, delay control, generate statement, event control, conditional statements, Multiway branching, loops, sequential and parallel blocks.
Useful Modeling Techniques: Procedural continuous assignments, overriding parameters, conditional compilation and execution, useful system tasks.
Logic Synthesis with Verilog/ VHDL: Logic Synthesis, Impact of logic synthesis, Verilog/ VHDL Synthesis, Synthesis design flow, Verification of Gate-Level Netlist.

Text Book:

1. Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", Pearson Education, Second Edition.
2. James R. Armstrong and F. Gail Gray, VHDL Design Representation and Synthesis, Prentice Hall, 2000.

Reference Books:

1. Donald E. Thomas, Philip R Moorby, 'The Verilog Hardware Description Language", Springer Science-Business Media, LLC, Fifth edition.
2. Michael D. Ciletti, "Advanced Digital Design with the Verilog HDL" Pearson (Prentice Hall), Second edition.
3. Padmanabhan, Tripura Sundari, "Design through Verilog HDL", Wiley, 2016.
4. A.M. Dewey, Analysis and Design of Digital Systems with VHDL, PWS Kent, 1996.

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PE 2	EI6242	VLSI Design Verification and Testing	3	0	0	3

Course Outcomes: At the end of the course the student will be able to

1. Outline the concepts of verification methodologies.
2. Acquire knowledge on DFT for complex circuit analysis.
3. Analyse on Various Verification Techniques Employed for Verifying VLSI Chips.

MODULE-I

Scope of testing and verification in VLSI design process. Issues in test and verification of complex chips, embedded cores and SOCs. Fundamentals of VLSI testing. Fault models. Automatic test pattern generation.

MODULE-II

Design for testability. Scan design. Test interface and boundary scan. System testing and test for SOCs. Iddq testing. Delay fault testing. BIST for testing of logic and memories. Test automation.

MODULE-III

Design verification techniques based on simulation, analytical and formal approaches. Functional verification. Timing verification. Formal verification. Basics of equivalence checking and model checking. Hardware emulation.

References:

1. M. L. Bushnell and V.D. Agrawal, *Essential*s *of Electronic Testing for Digital Memory and Mixed Signal VLSI Circuits*, Springer, 2005
2. H. Fujiwara, Logic Testing and Design for Testability, MIT Press, 1985
3. M. Abramovici, M. Breuer, and A. Friedman, *Digital System Testing and Testable Design*, IEEE Press, 1994
4. M. Huth and M. Ryan, Logic in Computer Science, Cambridge Univ. Press, 2004
5. T. Kropf, Introduction to Formal Hardware Verification, Springer Verlag, 2000

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PE 2	EI6244	Mixed Signal & RF IC Design	3	0	0	3

Course outcomes: After completion of the course, the students will be able to

1. Apply the RF and Mixed signal design concepts
2. Analyze biasing, feedback, and noise.
3. Design a RF amplifier, Power amplifier, LNA.

Module I

Introduction: Basic Concepts in RF Design, Passive RLC Networks, Passive IC Components, and Their Characteristics.

Voltage References & Biasing: Supply Independent Biasing,

Feedback Systems: De-sensitivity, Stability, Errors, Compensation.

Noise: Thermal noise, Shot Noise, Popcorn Noise, and Flicker Noise in devices and circuits.

Module II

Basic concepts of wireless communication systems design, transceiver architectures, design flow for RF and mixed-signal circuits and systems, technological issues related to CMOS-based RF circuits;

On-chip transmission lines and their properties, modeling of lumped and distributed RF circuits; On-chip CMOS low noise amplifiers, power amplifiers, mixers, detectors and switches;

Module III

A brief review of S/H characteristics and quantization noise, ADC and DAC specifications, ADC and DAC architectures, brief review of OP-AMP based ADC and DAC;

Ring oscillators, LC Oscillators, ring and LC oscillator-based voltage-controlled oscillators, simple PLLs, PLLs, delay locked loops.

Text Book:

1. T. H. Lee, “The Design of CMOS RF Integrated Circuits”, Cambridge University Press.
2. B. Razavi, “RF Microelectronics”, Pearson Education.

Reference Books:

1. B. Razavi, “Design of Analog CMOS Integrated Circuits”, Tata McGraw-Hill,2002.
2. Sorin Voinigescu, “High Frequency Integrated Circuits”, Cambridge University Press.
3. Reinhold Ludwig, Gene Bogdanov, “RF Circuit Design Theory and Applications”, Pearson Education.

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PE 2	EI6246	Low Power VLSI System	3	0	0	3

Course Outcomes: Upon completion of the course, the students will demonstrate the ability to:

1. Acquire the knowledge about various CMOS fabrication process and its modelling andinfer about the second order effects of MOS transistor characteristics.
2. Analyze and implement various CMOS low voltage and low power static logic circuits.
3. Learn the design of various CMOS low voltage and low power dynamic logic circuits.
4. Learn the different types of memory circuits and their design.
5. Design and implementation of various structures for low power applications.

Module I

Introduction: Sources of power dissipation, Static power dissipation, Active power dissipation. Circuit Techniques for Low-Power Design: Designing for low-power, Circuit techniques for leakage power reduction – Standby leakage control using transistor stacks, Multiple Vth techniques, Dynamic Vth technique, Supply voltage scaling technique.

Low- Voltage Low-Power Adders: Standard adder cells – Half adders, Full adders and their various schematic configurations, CMOS adder's architecture – Ripple carry adders, carry lookahead adders, Carry select adders, Carry save adders, Carry skip adders, Conditional sum adders.

Low- Voltage Low Power Multipliers: Overview of multiplication – Unsigned multiplication, Shift/add multiplication algorithms, Multiplication of signed numbers, Types of multipliers architecture – Serial multipliers, Parallel multipliers, serial-parallel multipliers, Braun multiplier, Baugh-Wooley multiplier, Booth multiplier, Wallace tree multiplier.

Module II

Performance valuation of various adder architectures: BiCMOS adders – PT-BiCMOS Gate, Low- voltage low-power design techniques – Trends of technology and power supply voltage, Low-voltage low-power logic styles, Current-mode adders – Current-mode CMOS adders using multiple-valued logic, SOI CMOS, Residue adders based on binary adders, Fast addition using single-digit number system.

Low-Voltage Low Power Read-Only Memories: Types of ROM, Basic physics of floating gate non- volatile devices, Floating gate memories, Basics of ROM – Chip architecture, ROM cell arrays, Low- power ROM Technology – Sources of power dissipation, Low-power techniques at architecture level, Low-power techniques at circuit level. Low-Voltage Low Power Static Random-Access Memories: Basics of SRAM, Memory cell, Pre-charge and equalization circuit, Decoder, Address transition detection, Sense amplifier, Output latch, Low-power SRAM technology – Sources of SRAM power, Development of low power circuit techniques.

Module III

Low-Voltage Low Power Static Random-Access Memories: Types of DRAM – Conventional DRAM, Fast page mode DRAM, Enhanced DRAM, Extended data out DRAM, Burst extended data output DRAM, Synchronous DRAM, Enhanced synchronous DRAM, Double data-rate DRAM, Synchronous link DRAM, Rambus DRAM, Direct Rambus DRAM, Video RAM, Embedded DRAM, Basics of DRAM, Self-refresh Circuit, Half-voltage generator, Back-bias generator, Boosted-voltage generator, Reference-voltage generator, Voltage-down converter. Large Low-Power VLSI System Design Applications: Behavioral level transform, Algorithm, and architecture level transforms for low power.

Text Books

1. Kiat-Seng Yeo and Kaushik Roy, "Low-Voltage Low-Power VLSI Subsystems", TMH Pvt. Ltd., 2009, ISBN-13: 978-0-07-067750-0, ISBN-10: 0-07-067750-6.
2. Kaushik Roy, Sharat C. Prasad, "Low-Power CMOS VLSI Circuit Design", Wiley India Pvt Ltd, 2009, ISBN: 812652023X, ISBN-13: 9788126520237, 978-8126520237.

Reference Books

1. Abdellatif Bellaouar and Mohamed Elmasry, "Low-Power Digital VLSI Design: Circuits and Systems," Springer, 1995.
2. Gary K. Yeap, "Practical Low Power Digital VLSI Design," Springer, 1998.

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Techno Campus, Mahalaxmi Vihar, Ghatikia, Bhubaneswar-751029.

Syllabus (Effective from 2023-24)

School/ Department: School of Electronic Sciences

Course: M. Tech., Programme: VLSI Design and Embedded Systems (VLSI),

Duration: 2 years (Four Semesters)

PE 3	EI6248	Hardware Software Co-design	3	0	0	3

Course Outcome:

1. **Define a concurrent specification from an algorithm, analyse its behaviour and partition the specification into software (C code) and hardware (HDL) components.**
2. **Describe the broad range of system architectures that currently exist and define their fundamental attributes including speed, energy, area, design complexity, design cost, etc.**
3. **Demonstrate the ability to translate between C code and VHDL by solving meaningful, real-world problems and then implementing and testing your solution on a FPGA SoC architecture.**

Module I

Co- Design Issues: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology. **Co- Synthesis Algorithms:** Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

Module II

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure. Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

Module III

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

TEXT BOOKS:

1. Jorgen Staunstrup, "Hardware / Software Co- Design Principles and Practice", Wayne Wolf – 2009, Springer.
2. Giovanni De Micheli, Mariagiovanna Sami, "Hardware / Software Co- Design", 2002, Kluwer Academic Publishers

REFERENCE BOOKS:

1. Patrick R. Schaumont, "A Practical Introduction to Hardware/Software Co-design", 2010, Springer

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Duration: 2 years (Four Semesters)

PE 3	EI6250	Hardware Security	3	0	0	3

Course Outcomes:

1. This course will focus on the importance of addressing different security threats on modern hardware design, manufacturing, installation, and operating practices.
2. In particular, the threats would be shown to be relevant at scales ranging from a single user to an entire nation & public infrastructure.
3. Through theoretical analyses and relevant practical world case studies, the threats would demonstrate, and then state-of-the-art defense techniques would be described.
4. The course would borrow concepts from diverse fields of study such as cryptography, hardware design, circuit testing, algorithms, and machine learning.

Module I

Overview of Different Issues of Hardware Security
Preliminaries: Algebra of Finite Fields, Basics of the Mathematical Theory of Public Key Cryptography, Basics of Digital Design on Field-programmable Gate Array (FPGA), Classification using Support Vector Machines (SVMs)

Module II

Useful Hardware Security Primitives: Cryptographic Hardware and their Implementation, Optimization of Cryptographic Hardware on FPGA, Physically Unclonable Functions (PUFs), PUF Implementations, PUF Quality Evaluation, Design Techniques to Increase PUF Response Quality Side-channel Attacks on Cryptographic Hardware: Basic Idea, Current-measurement based Side- channel Attacks (Case Study: Kochers Attack on DES), Design Techniques to Prevent Side-channel Attacks, Improved Side-channel Attack Algorithms (Template Attack, etc.), Cache Attacks. Testability and Verification of Cryptographic Hardware: Fault-tolerance of Cryptographic Hardware, Fault Attacks, Verification of Finite-field Arithmetic Circuits

Module III

Modern IC Design and Manufacturing Practices and Their Implications: Hardware Intellectual Property (IP) Piracy and IC Piracy, Design Techniques to Prevent IP and IC Piracy, Using PUFs to prevent Hardware Piracy, Model Building Attacks on PUFs (Case Study: SVM Modeling of Arbiter PUFs, Genetic Programming based Modeling of Ring Oscillator PUF) Hardware Trojans: Hardware Trojan Nomenclature and Operating Modes, Countermeasures Such as Design and Manufacturing Techniques to Prevent/Detect Hardware Trojans, Logic Testing and Side-channel Analysis based Techniques for Trojan Detection, Techniques to Increase Testing Sensitivity Infrastructure Security: Impact of Hardware Security Compromise
on Public Infrastructure, Defense Techniques (Case Study: Smart-Grid Security)

Text Books:

1. Debdeep Mukhopadhyay and Rajat Subhra Chakraborty, "Hardware Security: Design, Threats, and Safeguards", CRC Press

Reference Books:

1. Ahmad-Reza Sadeghi and David Naccache (eds.): Towards Hardware-intrinsic Security: Theory and Practice, Springer.

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Course: M. Tech., Programme: VLSI Design and Embedded Systems (VLSI),

Duration: 2 years (Four Semesters)

PE 3	EI6252	ASIC and SoC Design	3	0	0	3

Course Outcomes: At the end of the course, the student will be able to:

1. Generalize the basic concepts of CMOS logic cells and its ASIC libraries.
2. Acquire knowledge on UVM.
3. Understand the basic concept of SOC design and verification.
4. Acquire knowledge on Low power design.

MODULE – I

Introduction to ASIC, ASIC product framework, Methodology and Design Flow, FPGA to ASIC Conversion, Gate array architecture, cell-based architecture.

Universal verification methodology: Introduction, Polymorphism, Hierarchy of UVM, Library, Communication protocol, System Verilog functional. Clock Domain verification, Static Verification.

MODULE – II

SoC Design and Verification: Introduction, Design for Integration, SoC Verification, Set-Top-Box SoC, Set-Top-Box SoC Example. Voice Over IP network SoC verification.

Physical Design: Introduction, Overview of Physical Design Flow, Some Tips and Guidelines for Physical Design, Modern Physical Design Techniques.

MODULE – III

Low-Power Design: Introduction, Power Dissipation, Low-Power Design Techniques and Methodologies, Low-Power Design Tools, Tips and Guidelines for Low-Power Design.

Text Books:

1. Farzad Nekoogar and Faranak Nekoogar, From ASICs to SoCs: A Practical Approach, Pearson Education, 2003, ISBN-10: 0-13-033857-5, ISBN-13: 978-0- 13-033857-0

Recommended Reading:

1. Michael Smith, Application Specific Integrated Circuit, Addison-Wesley, 1997, ISBN:0201500221
2. Jari Nurmi, Processor Design: System-On-Chip Computing for ASICs and FPGAs, Springer, 1st edition, 2007, ISBN: 1402055293
3. Douglas J. Smith, HDL Chip Design – a practical guide for designing, synthesizing and simulating ASICs and FPGAs using VHDL or Verilog, Doone Publications, 2000, ISBN: 0965193438

OE 1	Any One from the List of OE 1 (Appendix-I)	3	0	0	3

Refer Appendix-I for detailed Syllabus.

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PR 1	EI6642	Project (Specialization Related)	0	0	4	2

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Duration: 2 years (Four Semesters)

LC 3	EI6542	Embedded System and HDL Lab	0	0	4	2

Using AT89C51/ ARM/ Keil programming

Course Outcomes: On completion of this lab course the students will be able to:

1. Understand the hardware-based design on ARM processor.
2. Demonstrate a clear Understanding in hardware design language Verilog/ VHDL and simulate and synthesize circuits
3. To analyse the results of logic and timing simulations and to use these simulation results to debug digital systems.
4. Model a Combinational/ Sequential circuit using hardware description language Verilog/VHDL and validate its functionality

List of Experiments using ARM

1. Write a simple program for arithmetic operations – addition, subtraction, multiplication and division of 16 or 32 – bit numbers
2. Flashing of LEDs and Interfacing 7-Segment LED
3. Interfacing ADC, DAC
4. Interfacing of Analog Key pad, on board push button
5. Interfacing stepper motor.
6. Interfacing temperature sensor.
7. Interfacing Bluetooth module.
8. Interfacing Real Time Clock
9. Interfacing of micro–SD Card.
10. Interfacing Wi-Fi Module

List of Experiments using HDL (VHDL/ Verilog)

11. Design of Decoder, Encoders, Mux, Demux.
12. Code Converter, parity generator (with for loop and Generic statements).
13. Design of all type of Flip-Flops using (if-then-else) Sequential Constructs
14. Design of Shift Registers, universal shift registers, counters.
15. Design of Barrel Shifters, Digital Multipliers

AC 2	Any One from the List of AC 2 (Appendix-I)	2	0	0	0

Refer Appendix-I for detailed Syllabus.

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Course: M. Tech., Programme: VLSI Design and Embedded Systems (VLSI),

Duration: 2 years (Four Semesters)

3rd Semester

PE 4	EI7241	Semiconductor Device Modeling and Simulation	3	0	0	3

Course Outcomes: By the end of the course, students should be able to:

1. Understand the basic concepts of PN junction-based device.
2. Acquire the concept of field effect transistors.
3. Learn the modelling of SPICE based device.
4. Design and implement various structure for numerical simulation.

Module-I:

Semiconductor electronics: Physics of Semiconductor Materials, Band Model of Solids, Thermal-Equilibrium Statistics, Carriers in Semiconductors, Drift Velocity, Mobility and Scattering, Drift & Diffusion Current, Hall-Effect.
Metal-Semiconductor contacts and PN junctions: Metal Semiconductor junctions, Current-Voltage Characteristics, Surface Effects. The PN junction, Step Junction, Linearly Graded junction, Heterojunctions, Reverse-Biased PN junctions and breakdown mechanism. Generation and Recombination.

Module-II:

MOSFETs Physical Effects and Models: MOS Capacitor, Flat Band Voltage, Oxide and Interface Charge, High and Low Frequency C-V Characteristics: Charge- Coupled Devices, non-volatile memory. Basic MOSFET behavior, MOSFET scaling and short channel behavior. Complementary MOSFETs (CMOS), electric fields and velocity-saturation, basic leakage currents, channel length modulation, body bias effect, threshold adjustment, sub-threshold conduction.
Short Channel Effects: Limitation of long channel analysis, short-channel effects: velocity saturation, device degradation, channel length modulation, body bias effect, threshold adjustment, mobility degradation, hot carrier effects, MOSFET scaling goals, gate coupling, velocity overshoot, high field effects in scaled MOSFETs, substrate current and other effects in scaled MOSFETS.

Module-III:

Modeling: SPICE transistor modeling, compact MOSFET modeling approaches, physics of nanoscale MOSFET, and Design issues of nanoscale MOSFET: challenges of nanoscale MOSFET, scaling trends of MOSFETs, issues for nanoscale MOSFETs (short channel effects), key issues in modeling of MOSFET.
Numerical Simulation: Importance of semiconductor device simulators -Key elements of physical device simulation, Introduction to the TCAD Simulation Tool, Examples of TCAD Simulations –MOSFETs and SOI

Text Books:

1. Advanced Semiconductor Devices by Taur and Ning.
2. Device Electronics for Integrated circuits by Muller and Kammins.

Reference Books:

1. Physics of Semiconductor Devices by S. M. Sze and Kwok K. Ng, 3rd Edition,(John Wiley & Sons, 2002).
2. Semiconductor Physics and Devices by Donald A. Neamen, 3rd Edition, McGraw Hill, 2003

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Course: M. Tech., Programme: VLSI Design and Embedded Systems (VLSI),

Duration: 2 years (Four Semesters)

PE 4	EI7243	Nanomaterials and Nanotechnology	3	0	0	3

Course Outcomes: At the end of the course the student will be able to

1. Understand the physical concept of Nanomaterials.
2. Analyze the different synthesis and characterization technique used for nanoparticles.
3. Understand the concept and application on various nanodevices.

MODULE-I:

Introduction

Introduction of nano materials and nanotechnologies, Features of nanostructures, Applications of nanomaterials and technologies, Nano dimensional Materials 0D, 1D, 2D structures, Size Effects, Fraction of Surface Atoms, Specific Surface Energy and Surface Stress, Effect on the Lattice Parameter, Phonon Density of States, the General Methods available for the Synthesis of Nanostructures, precipitative, reactive, hydrothermal/solve thermal methods, suitability of such methods for scaling, potential Uses.

MODULE-II:

Electronic and Optical properties of nanostructures. Energy sub-bands. Electron transport in two –dimensional electron gas (density of states), Carrier scattering, resistance of a ballistic conductor, Transmission probability calculation, Electron tunneling, Resonant tunneling, Coupled nanoscale structures, and Superlattices.

Nanoparticle synthesis and Characterization:

Nanotechnology: Deposition techniques for Nanoscale Devices, Nanolithography, Self-Assembly Techniques, Brief introduction to Nanomaterials: Nanoparticles, Nanowires, Nanomagnetic Materials, Nanostructure Surfaces). Brief idea about characterization technique: The Atomic Force Microscope (AFM), Scanning Tunnelling Microscope, X-ray diffraction (XRD), Scanning electron microscopy (SEM).

MODULE-III:

Shrink-down approaches: Electronic devices Based on Nanostructures: Advance Heterostructure Devices, Downscaling of the MOSFET. Nanoscale FET Transistors, Resonant Tunneling Devices and Circuits, Single Electron Transistor and Related Devices. Devices based on carbon nanotubes, Optoelectronic Devices using Nanostructures: Quantum well and Quantum Dot LASERS, Quantum Cascade LASER, Quantum well-infrared photodetector, Superlattice LASER.

TEXT BOOKS:

1. I Gusev and A A Rempel, “Nanocrystalline Materials”, Cambridge International Science Publishing, 1st Indian edition by Viva Books Pvt. Ltd. 2008.
2. Introduction to Nanotechnology, C.P. Poole Jr., F.J. Owens, Wiley (2003).

REFERENCE BOOKS

1. Bharat Bhushan, “Springer Handbook of Nanotechnology”, Springer, 3rd edition, 2010.
2. Karl Goser, “Nanoelectronics and Nanosystems,” Springer, 2004

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School/ Department: School of Electronic Sciences

Course: M. Tech., Programme: VLSI Design and Embedded Systems (VLSI),

Duration: 2 years (Four Semesters)

PE 4	EI7245	Micro Electromechanical Systems	3	0	0	3

Course Outcomes: At the end of the course, the student will be able to**:**

1. Understand the purpose of MEMS and their application areas.
2. Choose appropriate microfabrication technology for a specific application.
3. Choose appropriate nanofabrication technology for a specific application.
4. Select one or more suitable MEMS integration and packaging approaches for a given application.

Module-I:

Intrinsic Characteristics of MEMS: Miniaturization, Microelectronics Integration, Mass Fabrication with Precision, Microelectronics Fabrication Process, Silicon based MEMS processes.

Electrostatic Sensing and Actuation: Introduction to Electrostatic Sensors and Actuators, Parallel-Plate Capacitors, Applications of Parallel Plate Capacitors, . Thermal Sensing and Actuation: Introduction, Sensors and Actuators Based on Thermal Expansion, Thermal Couples, Thermal Resistors, Applications. Magnetic Actuation.

Module-II:

Piezoresistive Sensors: Piezoresistive Sensor Materials, Stress Analysis of Mechanical Elements, Applications of Piezoresistive Sensors. Piezoelectric Sensing and Actuation: Introduction, Properties of Piezoelectric Materials, Applications.

Bulk Micromachining and Silicon Anisotropic Etching: Introduction, Anisotropic Wet Etching, Dry Etching of Silicon-Plasma Etching, Deep Reactive Ion Etching (DRIE), Isotropic Wet Etching, Gas-Phase Etchants, Native Oxide, Wafer Bonding.

Surface Micromachining: Basic Surface Micromachining Processes, Structural and Sacrificial Materials, Acceleration of Sacrificial Etch, Stiction and Anti-Stiction Methods, Assembly of 3D MEMS, Foundry Process.

Module-III:

Optical MEMS: Passive MEMS Optical Components-Lenses, Mirrors, Actuators for Active Optical MEMS Actuators for Small Out-of-Plane Translation, Actuators for Large In Plane Translation Motion, Actuators for Out-of-Plane Rotation.

Polymer MEMS: Introduction, Polymers in MEMS- Polyimide, SU-8, Liquid Crystal Polymer (LCP), PDMS, PMMA.

Text Books

1. Chang Liu, Foundations of MEMS, Pearson Education Inc., 2012.
2. Stephen D Senturia, Microsystem Design, Springer Publication, 2000.

Reference Books

1. Tai Ran Hsu, MEMS & Micro systems Design and Manufacture, TMH, New Delhi, 2002.

PR 2	EI7641	Dissertation (Phase-I)	0	0	24	12

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Course: M. Tech., Programme: VLSI Design and Embedded Systems (VLSI),

Duration: 2 years (Four Semesters)

4th Semester

PR 3	EI7642	Dissertation (Phase-II)	0	0	32	16